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(71) Applicant: SUPERMAC TECHNOLOGY [US/US]; 485 Potrero Avenue, Sunnyvale, CA 94086 (US).

(72) Inventor: GILBERT, Douglas, J. ; 3933 California Way, Livermore, CA 94550 (US).

(74) Agents: EQUITZ, Alfred, A. et al.; Limbach & Limbach, 2001 Ferry Building, San Francisco, CA 94111 (US).

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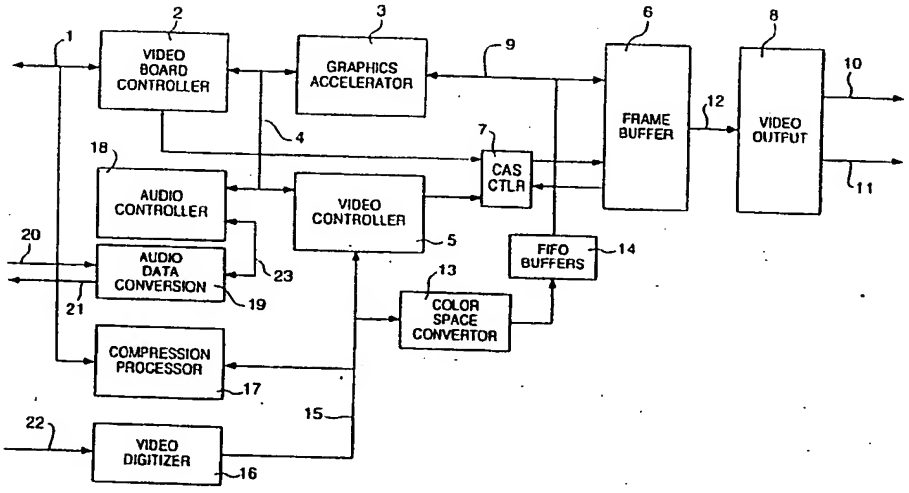

(57) Abstract

An apparatus for the manipulation and display of digital video and audio includes a plug-in board for a personal computer and provides real-time digital video and audio digitization. The video is digitized by a video digitizer (16) and converted to RGB, compressed using a hardware compression processor (17), and written to the computer system disk, capturing the video in real-time. Concurrent to the video capture, an audio data convertor (19) digitizes two channels of audio (20). This data is buffered in RAM memory on the board, where it can then be transferred to the computer system disk. The board also supports the playback of video and audio at real-time rates. Compressed video data is transferred from the computer system disk to the board, where it is decompressed by the compression processor (17).

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PERSONAL COMPUTER APPARATUS FOR DIGITAL VIDEO AND AUDIO MANIPULATION

FIELD OF THE INVENTION

This invention relates to the field of full motion video in a personal computer environment.

BACKGROUND OF THE INVENTION

Color images are generally represented in a computer environment with an independent color value for each pixel. Since the video displays used for computer displays utilize RGB (red, green, and blue) video signals, color image data is typically represented in an RGB format.

The data storage requirements for color images are fairly high. A single color image stored at conventional NTSC TV resolution (approximately 640 x 480) is almost one million bytes (assuming one byte is used for each of the red, green, and blue color components).

Although the manipulation of single color images is very useful, many applications utilize full motion video. The support of full motion video in a computer environment is a much more daunting task than either still computer images or conventional motion video because of the significant increase in both data storage and data bandwidth requirements.

Although different video standards specify different resolution and refresh rates, the American NTSC standard refresh rate is 29.94 Hz, thus a single second of NTSC video requires over 27 Mbytes if stored in the format described above.

These storage and bandwidth requirements are well beyond the capabilities of even the fastest current personal computers such as the Apple

Macintosh IIfx (Apple and Macintosh are trade-marks of Apple Computer Corporation).

Image compression technology has been developed recently to reduce the storage requirements of high resolution color images. Although the application of this technology to video has been speculated, the described embodiment is the first system to solve the problems associated with the integration of full motion video at full NTSC resolution in a personal computer environment.

Thus, an object of the invention is a system which can digitize and manipulate full motion, broadcast standard video in a cost effective personal computer environment.

Another object of the invention is a system which can digitize video, compress the digital video, and write the compressed video to disk, while maintaining full broadcast video resolution and frame rates.

Another object of the invention is a system which can generate video compatible with broadcast standards (such as NTSC and PAL) from compressed digital video stored on a disk system.

Another object of the invention is a system which can manipulate digital video and audio and maintain synchronization between the two.

SUMMARY OF THE INVENTION

Accordingly, a plug-in board for an Apple Macintosh II family personal computer system according to the present invention incorporates hardware and software to support broadcast standard video and audio digitization, manipulation, compression, decompression, and conversion back to analog. The board also contains a conventional frame

buffer and graphics controller, and will typically be used to drive the primary graphics display screen. The board connects to the Apple Macintosh II over the NuBus (NuBus is a trademark of Texas Instruments, Inc.).

Broadcast compatible video is sampled using analog to digital converters with a sample clock that is phase locked to the color burst signal in the input video signal. Video formats that can be handled include NTSC (the U.S. TV standard), PAL (the European TV standard), and S-VHS.

The video digitizer separates the chrominance components from the composite video signal, and, by using a decimation filter, reduces the bandwidth of the U and V chrominance components. The video digitization and chrominance separation can be handled by commercially available chip sets such as the Phillips TDA8709, TDA8708, SAA7191, and SAA7197 (Phillips is a trademark of Phillips Semiconductor).

The luminance and chrominance components are transferred over the pixel data bus (16 bits) at full video bandwidth to a JPEG image compression processor (such as the C-Cube CL550B, C-Cube is a trademark of C-Cube Microsystems) and to a color space converter (such as the Phillips SAA7192).

The color space converter converts the YUV color data from the pixel data bus to an RGB format so that it can be displayed on the computer display monitor. The RGB data is buffered using FIFOs to allow the pixel data to be synchronized to the frame buffer timing. RGB is transferred to the frame buffer so that the video being digitized can be displayed in a window on the display screen.

The frame buffer is controlled by a video board controller and graphics accelerator which support

standard graphics operations such as block transfers. These features are important to provide acceptable performance for operations other than the display of the digitized video.

The video board controller generates video timing for the broadcast standard video formats, as well as high resolution video formats which are commonly used in high-end personal computers.

As the video is being digitized and displayed in a window on the graphics display, it is also compressed by the JPEG compression processor. Since the JPEG standard operates on 8x8 pixel blocks, and operates on the color components independently, buffering must be provided for the digital video data. This is handled as part of the compression processor. The compression ratio that can be achieved by the compression processor varies based on the desired image quality and the particular image itself. Since the compressed video will typically be written to the hard disk system, the compression ratio will be adjusted to maintain an average compressed digital video bandwidth that is less than the sustained disk subsystem bandwidth. This is accomplished by buffering the compressed digital video data in main memory on the personal computer before transferring to disk, and adjusting the compression parameters on the compression processor such that the buffer does not overflow or empty. The buffer must be large enough to allow time for the compression parameters to be varied to adjust for the disk bandwidth.

Concurrently with the video processing described above, the board also handles audio digitization and controls transfer to the personal computer disk subsystem. Two channels of audio can be digitized.

The digitized audio is buffered by being stored in a relatively large RAM buffer. When the microprocessor in the personal computer is not operating on another command and when the RAM buffer starts to become full, the data is transferred from the buffer to the personal computer main memory and from there to the disk subsystem. The product also interleaves the audio data with the video data as it is written to the disk subsystem.

The description above discusses the operation of the invention while the system is capturing video and audio data and storing it on the personal computer disk subsystem. The invention is also designed to allow the video data and audio data to be edited and played back.

Since the video data is now stored on a random access storage system, it is possible to manipulate each frame of the video at non-real-time rates. This allows a system including the board of the present invention to be used as the heart of a very powerful video editing system. To edit a particular frame, the compressed digital video data corresponding to the frame is read from the computer disk subsystem and transferred to the compression processor. The image is decompressed and transferred over the pixel data bus and then over the NuBus back to main system memory. Once there, it can be manipulated in any desired manner by any available general image processing, graphics editing, and paint system applications software. After the editing on the frame has been completed, the image is transferred back to the compression processor over the NuBus and pixel data bus, where it is recompressed and transferred back to the disk subsystem. It is also possible to edit the frame directly in the frame

buffer since the frame buffer can be accessed as system memory.

The stored and edited video and audio data can be played back at real-time rates, allowing it to be previewed in a window on the computer's graphics display or be converted to composite or component video and be displayed on a conventional TV screen, or recorded to video tape.

The disk file containing the compressed video and audio data is read from the personal computer disk subsystem into a large RAM buffer in the computer system main memory. The buffer must be large enough to allow variations in the disk read speed and compressed video bandwidth requirements to be averaged out. The compressed video data is transferred to the compression processor over the NuBus.

The data is decompressed by the compression processor, and transferred over the pixel data bus to the color space converter. The color space converter transforms the pixel data from YUV to RGB. The RGB data is written to the frame buffer after buffering in the FIFOs as described above. For previewing, the RGB digital video is displayed in a window on the display. To generate full resolution broadcast compatible full motion video, the video timing of the frame buffer can be changed to be compatible with a specified video standard. The digital video data from the frame buffer is converted to analog, and then converted to a composite or S-VHS component signal as appropriate.

Concurrently with the output of the video data, the audio data is transferred from the computer's disk subsystem through a RAM buffer in main memory to the RAM buffer on the board. The digital audio data

is then converted to two channel analog signals and output to a speaker system.

These and other objects and features of the present invention will be understood more fully from the following detailed description which should be read in light of the accompanying drawings in which corresponding reference numerals are discussed in the text, and refer to corresponding parts throughout several views.

BRIEF DESCRIPTION OF THE FIGURES OF THE DRAWING

Figure 1 is an overall functional block diagram of the preferred embodiment of the invention.

Figure 2 is a block diagram of a personal computer system incorporating the present invention, showing the digital video board-plugged into a conventional personal computer.

Figure 3 is a block diagram showing additional detail of the video digitizer.

Figure 4 is a block diagram showing additional detail of the compression processor.

Figure 5 is a block diagram showing additional detail of the video output.

Figure 6 is a block diagram showing additional detail of the audio controller.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figure 2, the preferred embodiment of the invention is a digital video board 30, that is coupled to transmit signals to and receive signals from the NuBus expansion bus 35 on an Apple Macintosh II computer system. The microprocessor 31 is the central processing unit that controls the operating system and the applications program which directs the operation of the digital video board. In the Apple

Macintosh II family, the microprocessor 31 is a Motorola 68020, 68030, or 68040 (Motorola, 68020, 68030, and 68040 are trademarks of Motorola Semiconductor, Inc.). Other microprocessors such as the Intel 80x86 family (Intel is a trademark of Intel Corporation), SPARC (SPARC is a trademark of Sun Computer, Inc.), or MIPS (MIPS is a trademark of MIPS Computer Corporation) could also be used as the central processor in the system.

The main memory 32 stores the programs and data sets upon which the microprocessor 31 operates. The mass storage device 33 (personal computer disk subsystem) is typically a hard disk, but could also be a magneto-optical disk or other read/write device. The invention can also be used with a read-only device, such as a CD ROM.

The microprocessor 31, mass storage devices 33 and main memory 32 communicate with each other over the system bus 34. The system bus 34 and an expansion bus 35 are coupled to exchange data. In the Apple Macintosh II family of personal computers, the expansion bus 35 adheres to the NuBus standard. Additional information on the NuBus operation is available from Texas Instruments, Dallas, Texas.

A more detailed functional block diagram of the digital video board 30 of the present invention is shown in Figure 1. Referring to Figure 1, the video board controller 2 and the compression processor 17 connect to the NuBus (not shown) over bus extension 1. This allows the digital video board to receive commands from the microprocessor 31 (Figure 2), and allows the microprocessor 31 to read data from and write data to the on-board registers and memory.

The NuBus control signals are also supported by the video board controller. In the preferred embodiment, the video board controller is implemented as an ASIC (Application Specific Integrated Circuit). However, the functions implemented by the present invention can be implemented with commodity VLSI components. An example of a NuBus video card implemented using commodity components is described in "Designing Cards and Drivers for the Macintosh Family" published by Addison-Wesley Publishing Company, Inc, Reading, MA. The ASIC solution is preferred because of cost and board space constraints.

The digital video board of the present invention is generally used to drive a graphics display 36 in addition to handling digital video tasks. A graphics accelerator 3 is reciprocally coupled to the video board controller over a bus 4. The graphics accelerator 3 is also reciprocally coupled to a frame buffer 6 over a bus 9. The frame buffer 6 stores information for 512K pixels which supports a maximum display resolution of 832 x 624 pixels. This resolution can be increased following practiced methods. Each pixel in the frame buffer contains eight bits for each of the red, green, and blue color components. Two additional bit planes are provided for mask and overlay functions, not directly pertinent to this invention. The operation of these additional bit planes is described in copending U.S. patent application _____.

The control logic to control the frame buffer video timing and memory control signals is contained in the video board controller 2. The frame buffer 6 generates digital video data 12 and is coupled to be continuously read by a video output circuit 8 over a

bus 12. The video output circuit 8 is coupled to provide video signals for updating the display screen 36 (Figure 2). The video output circuit 8 converts the digital video data into analog signals 10 to drive the display monitor 36. A separate set of analog outputs 11 is generated which is designed to drive composite video devices such as video tape recorders (not shown).

The graphics accelerator 3 controls the frame buffer data path. This function is preferably implemented in a single ASIC, and is similar to devices that are well known in the art for high performance graphics systems. The bus 9 between the graphics accelerator and the frame buffer supports 96 bit transfers. This allows four pixels to be transferred to or from the graphics accelerator 3 every bus cycle, thereby providing increased performance for moving pixels around on the display screen.

The functions performed by the remainder of the functional blocks shown in Figure 1 are described below with respect to the common audio/video operations that will be performed using the invention.

Importing Video

The first step in the processing of video images on a personal computer is to import the video data into the system. Since the video data is digitized and stored on the mass storage device 33 (Figure 2), inputing video signals is referred to as video capture. Referring to Figure 1, the video data is coupled to the board over a bus 22 and is processed and digitized by the video digitizer circuit 16. The preferred embodiment supports a variety of video

formats including NTSC, PAL, and S-VHS. Although not supported by the preferred embodiment, SECAM, HDTV and other high resolution video standards can be supported by other embodiments using the concepts taught by the present invention.

Referring to Figure 3, the transferred video data over input bus 22 is comprised of several different signals. The video digitizer 16 can switch between three video sources. The video input bus is coupled to two analog to digital converters 40 and 41. Each of the converters 40 and 41 are coupled to provide digital signals to a digital multistandard decoder 42. A clock generator 43 is coupled to provide a clock signal to each of the converters 40 and 41 and the decoder 42.

A first analog to digital converter 41 selects between two independent composite video inputs 46 and 47, and the luminance channel 45 of an S-VHS input. The composite inputs can be either NTSC or PAL standard. In the preferred embodiment, this first analog to digital converter 41 is implemented with a Phillips TDA8708 (Phillips is a trademark of Phillips Semiconductor).

If an S-VHS signal is used as the input, the first analog to digital converter 41 samples only the luminance signal 45. A second analog to digital converter 40 is used to sample the chrominance signal 44. This second analog to digital converter 40 is implemented with a Phillips TDA8709.

The analog to digital converters 40 and 41 generate digital samples corresponding to the analog input signal(s). A sample clock signal is generated by clock generator 43. The clock is phase locked to the color burst signal that is part of the input video signal. This allows the video signal to be

sampled appropriately to separate the chrominance signals from the luminance signal in the composite video inputs, and to split the two chrominance signals in the S-VHS chrominance input. In the preferred embodiment, the clock generator 43 is implemented with a Phillips SAA7197.

The digitized video samples are coupled to the digital multistandard decoder 42 which separates the chrominance and luminance color components, controls the video timing of the incoming video signal, and drives the pixel data bus 15 with separated YUV digital video data. The digital multistandard decoder 42 is implemented with a Phillips SAA7191 in the preferred embodiment.

Other equivalent or similar circuitry could be used for all or part of the video digitization function just described. The use of the four Phillips parts and the associated circuitry is described in the "Video Data Handbook" available from Phillips Semiconductors, Eindhoven, The Netherlands.

The output of the digital multistandard decoder 42 drives the pixel data bus 15 with 16 bit pixels in a YUV format. The data is in scan-line order, with timing determined by the particular video format of the sampled analog video.

Referring to Figure 1, as the video signal is being digitized, the application has the option to display the incoming video signal in a window (a rectangular region) on the computer display monitor 36. However, since the display monitors typically used for computer display purposes (such as those available from SuperMac Technology) are controlled via RGB video signals, the YUV video signals on the pixel data bus must first be converted to RGB. This is done using a color space converter 13. The video

digitizer 16 is coupled to provide signals to the color space converter 13, the video controller 5 and a compression processor 17 via the pixel data bus 15.

The color space converter transforms YUV data to RGB data in real time as the video data is digitized. The color space converter 13 of the preferred embodiment is implemented with a Phillips SAA7192, although other equivalent or similar circuitry could also be used for this function. The use of this part and associated circuitry is described in the "Video Data Handbook" referenced above.

The color space converter 13 is coupled to provide RGB signals to FIFO buffers 14 which are coupled to provide the RGB signals to the graphics accelerator 3 and the frame buffer 6. The data on the pixel data bus 15 is synchronous to the incoming video signal 22. However, this signal is asynchronous to the frame buffer 6 and the video board controller 2. To write the RGB data from the color space converter 13 into the frame buffer 6, the data must be resynchronized to the frame buffer clock. This is accomplished using the FIFO buffers 14. The FIFO buffers are implemented with industry standard 1K x 9 FIFO ICs, such as the CY425 available from Cypress Semiconductor, San Jose, CA, in the preferred embodiment.

The use of FIFO components of this type for data synchronization is well known in the art. To transfer the data from the FIFOs 14 to the frame buffer 6, the block pixel move mechanism in the graphics accelerator 3 is employed. Block pixel move is a common technique used in graphics displays to rearrange pixels on the screen, but has not previously been applied to the display of full-motion video windows. Pixels are first read from the FIFO

buffers 14 into the graphics accelerator 3 over the frame buffer data bus 9. They are then written back over the frame buffer data bus into the frame buffer 6. By transferring the data in this manner, the same logic can be used for updating the video window as is already necessary for high speed block pixel moves. The data can be moved directly from the FIFO buffers 14 to the frame buffer 6, but this is not preferred because of the additional control logic that would be required. The use of the pixel block move logic also allows the video window to be placed anywhere on the computer display screen. It is also possible to scale the size of the video window that is displayed, as is described in copending U.S. patent application _____.

The transfer over the pixel data bus 15 to the color space converter 13, and the transfer to the FIFO buffers 14, is controlled by the video controller 5. The video controller 5 is reciprocally coupled to the video board controller 2, the graphics accelerator 3 and an audio controller 18.

Although the digital video board of the present invention can be used to simply display an incoming video signal in a window on a personal computer display screen, a primary object of the invention is to store the incoming video in a digital format on a mass storage device so that it can be later recalled, edited, and output to a video display or video tape recorder, or recorded on a digital video storage media such as CD-ROM.

Referring to Figure 1, the digital video data is transferred from the video digitizer 16 to the compression processor 17 over the pixel data bus 15. The extension bus 1 is also reciprocally coupled to the compression processor 17. Additional detail of

the compression processor is shown in Figure 4. Referring to Figure 4, the RGB data from the pixel data bus 15 is reciprocally coupled to line re-sequencing buffer 48 and the JPEG processor 49. The line re-sequencing buffer 48 is used to allow the pixel data to be transferred from the video digitizer in scan-line order (the order in which it is represented in the incoming video signal) and transferred to the JPEG processor 49 in 8 x 8 pixel blocks. This latter ordering is required by the JPEG compression standard implemented by the preferred JPEG processor. The JPEG processor 49 of the preferred embodiment is implemented with a C-Cube CLS50B, although other equivalent or similar circuitry could also be used for this function. The use of this part and associated circuitry is described in the "CL550B JPEG Image Compression Processor" data book available from C-Cube Microsystems, San Jose, CA.

Referring to Figure 1, the compression processor 17 generates a compressed image data stream which is transferred over bus extension 1 to the NuBus expansion bus 35 (Figure 2). Referring to Figure 2, in the preferred embodiment, this transfer is accomplished via programmed operation of the microprocessor 31. The microprocessor reads the compressed image data from digital video board 30. It then writes the data into a memory buffer in main memory 32. At some later time, the data is transferred from the memory buffer to the mass storage device 33. This is accomplished via DMA (direct memory access) transfers or programmed I/O, depending on the type of personal computer into which the digital video board 30 is plugged into.

The use of the memory buffer in main memory is necessary to match the data rate from the compression processor 17 and to the mass storage device. It also allows time for the compression parameters in the compression processor 17 to be varied to match the average data rate with the average data rate available from the mass storage device. The compression ratio that can be achieved by the compression processor 17 varies based on the desired image quality and the particular image itself. By buffering the data, the compression parameters can be dynamically adjusted so that the memory buffer does not overflow or become empty.

Exporting Video

At some later time, it is desired that the compressed digital image data stored in the mass storage device 33 will be displayed on the computer video screen 36, or output to another video device such as a video tape recorder. Referring to Figure 2, the compressed image data is read from mass storage device and transferred to a buffer in main memory 32. At some later time, the microprocessor 31 reads the data from the main memory buffer and writes it to the digital video board 30.

Referring to Figure 1, compressed data is written to the compression processor 17 over bus extension 1. Referring to Figure 4, the JPEG processor 49 receives the compressed data and decompresses it into 8 x 8 pixel blocks in YUV format. The JPEG processor 49 is coupled to provide the YUV data to the line re-sequencing buffer 48. This data is transferred to the line re-sequencing buffer 48 where it can be read in scan-line order. The YUV data is transferred in scan-line order from

the line re-sequencing buffer over the pixel data bus 15 to the color space converter 13. The transfer over the pixel data bus 15 is controlled by the video controller 5.

The operations performed to transfer the YUV pixel data on the pixel data bus 15 to RGB pixels at the appropriate position in the frame buffer 6 are identical to those described above for importing video. To summarize, the color space converter 13 converts the YUV pixels to RGB. The RGB data is synchronized with the frame buffer timing in FIFO buffers 14, and is then transferred to the frame buffer 6 via the graphics accelerator 3.

The frame buffer 6 is implemented with industry standard 128K x 8 video RAMs, such as the NEC uPD42275, available from NEC Electronics, Mountain View, CA (NEC is a trademark of NEC Electronics) in the preferred embodiment. These video RAMs (VRAMs) incorporate a 256 x 8 SRAM which can be parallel loaded with a row from the internal DRAM memory array. Once loaded, the data contained in the SRAM can be shifted out a separate "serial" port to generate video for the display. Four VRAMs are used for each of the red, green and blue frame buffer banks. These four VRAMs provide four pixels in parallel from the serial ports, and therefore only need to be strobed with a clock pulse at one-fourth the pixel clock rate.

The SRAM reload and shifting operations are controlled by the video board controller 2. Referring to Figure 5, the RGB data from the frame buffer serial port 12 (Figure 1) is coupled to receive data from the frame buffer 6 (Figure 1). A shift register 52 is coupled to receive data from the port 12 and is coupled to provide data to a

RAMDAC 50. The RGB data is loaded into a shift register 52, which shifts the video data out, one pixel at a time, at the pixel clock rate to the RAMDAC 50 (RAMDAC is a trademark of Brooktree Corporation). The RAMDAC converts the digital data to analog and, in the preferred embodiment, is implemented with a Brooktree Bt473, although other equivalent or similar circuitry could also be used for this function (Brooktree is a trademark of Brooktree Corporation). The use of this part and associated circuitry is described in the "Brooktree Product Data Book" available from Brooktree Corporation, San Diego, CA.

The RAMDAC 50 generates three analog signals to drive the red, green, and blue video signals 10 to the display screen 36. These signals are also coupled to the RGB to NTSC/PAL encoder 51 which converts the RGB video signals 10 to composite video and S-VHS video signals 11. To generate NTSC, PAL, or S-VHS video, the video timing form the video board controller 2 is programmed for the appropriate video timing. The RGB to NTSC/PAL encoder 51 is implemented with a Motorola MC1377, although other equivalent or similar circuitry could also be used for this function. Additional information on the use of this part is available from Motorola Incorporated, Phoenix, AZ.

Editing Video

Video editing is accomplished one frame at a time. Any operation that can be performed on a pixel image can be performed on the video. Since the editing operations do not have to be performed in real time, the video editing options are virtually

unlimited. This section describes the operations that are performed to edit a video frame.

Each video frame is stored individually in compressed format, typically in a large data file containing numerous such frames, as well as audio information. It should be noted, however, that future image compression technologies may take advantage of interframe coding techniques which may require multiple frames to be decoded in order to regenerate a particular frame image. This invention does not preclude the use of these compression technologies. Referring to Figures 1, 2, and 4, the selected video frame is read from the file stored in the mass storage device 33 and, as with exporting video, is transferred to the digital video board 30 via a buffer in main memory 32. The compressed data is transferred to the compression processor 17 over bus extension 1. The JPEG processor 49 receives the compressed data and decompresses it into 8 x 8 pixel blocks in YUV format. This data is transferred to the line re-sequencing buffer 48 where it is then read in scan-line order back to the microprocessor 31 by transferring the YUV pixels over the pixel data bus 15 to the video controller 5, and then through the video board controller 2. This does not preclude one from transferring RGB pixels to simplify software. The transfer over the pixel data bus 15 is controlled by the video controller 5.

The microprocessor then converts this data from YUV to RGB using a software based algorithm and perform some editing function on the data. Between processing steps, the data is stored in buffers that are located in the main memory 32. The results of these processing steps may also be displayed on the display screen 36. This is accomplished by the

microprocessor under program control by writing pixel data to the frame buffer 6 using the video board controller 2 and the graphics accelerator 3.

After completing the processing of a video frame, the video frame will normally be recompressed and written to another file on the mass storage device 33. This is done by performing the reverse operations from those described above. Referring to Figures 1, 2, and 4, the image is converted to YUV (if it isn't already in this form) by the microprocessor 31. The YUV image is written into the line re-sequencing buffer 48 by transferring the data over the NuBus 35, over bus extension 1, through the video board controller 2, and the video controller 5, and over the pixel data bus 15. The transfer over the pixel data bus 15 is controlled by the video controller 5.

The JPEG processor 49 reads the image out of the line re-sequencing buffer 48 in 8 x 8 pixel blocks. The microprocessor 31 reads the compressed image data stream from the JPEG processor over bus extension 1, then over the NuBus 35, and writes the data to a memory buffer in the main memory 32. The data is then transferred to the mass storage device 33.

Audio Processing

The digital video board 30 is also designed to provide audio input and output concurrently with video I/O. Two channels of audio input and output are provided. In some ways, audio processing is more difficult than video processing, since it is continuous and any interruption in the data flow will cause undesirable artifacts in the reproduced sound.

Although not mandated by the hardware, audio input will typically occur concurrently with video input, and audio output with video output. Since the audio, as with the video, is digitized and stored on the mass storage device, audio input is referred to as audio importing. Likewise, audio output is referred to as audio exporting. The audio hardware is described with respect to the audio import and export operations in the next two sections.

Audio Importing

Referring to Figure 1, the two channel audio input 20 is coupled to the audio data conversion function 19. In the preferred embodiment, audio data conversion is implemented with the Sony CXD1077M, although other equivalent or similar circuitry could also be used for this function (Sony is a trademark of Sony Corporation). More information on this part is available from Sony Corporation, Tokyo, Japan.

The audio data converter 19 is reciprocally coupled to the audio controller 18. The audio data converter 19 converts the two analog data channels to digital data. This data is transferred to the audio controller 18 over the serial digital audio data bus 23.

Referring to Figure 6, the audio controller 18 includes a sound controller ASIC 53 reciprocally coupled to a buffer RAM 54. The buffer RAM 54 is actually implemented using an industry standard 4K x 9 FIFO, such as the IDT7204, available from Integrated Device Technology, Inc., Santa Clara, CA. The digital audio data is stored in this buffer until it can be read by the microprocessor 31 when it has some available time. By providing a large buffer, a large number of audio samples can be buffered,

allowing the microprocessor 31 to service the audio controller 18 during idle cycle times. The sound controller ASIC 53 converts the serial data stream from the audio data converter 19 into nine bit quantities for storage in the FIFO 54.

When the microprocessor 31 has available time, it reads the audio data from the buffer 54 through the sound controller ASIC 53 through the video board controller 2 and over the NuBus 35. The sound controller ASIC 53 groups the nine bit quantities stored in the buffer 53 into 32-bit words to match the data width of the rest of the system. The audio data is transferred into a memory buffer in main memory 32 where it is typically combined with the video data and written to a file on the mass storage device 33.

Audio Export

Audio export is the reverse of the audio import operations. Referring to Figures 1 and 2, the digital audio data is preferably interleaved with compressed video data in a file on the mass storage device 33. The data is read from the mass storage device and written to a buffer in main memory 32. As required by the audio output hardware, the microprocessor 31 reads audio data from the memory buffer in main memory and writes it to the audio buffer on the digital video board 30.

Referring to Figures 1, 2, and 6, the data is transferred over the NuBus 35 and over the bus extension 1 to the digital video board 30. From the bus extension, the audio data passes through the video board controller 2 and to the sound controller ASIC 53. The sound controller ASIC breaks the 32-bit

transfers into nine bit groups to store in the FIFO buffer 54.

As required by the audio data converter 19 the sound controller ASIC 53 reads data from the FIFO Buffer 54 and converts it to a serial bit stream to pass over the serial digital audio data bus 23 to the audio data converter. The audio data converter generates two channels of analog audio 21 which can be used to drive loudspeakers or be recorded with the video on video tape or some other audio/video media.

General

While the foregoing invention has been described with reference to its preferred embodiment, various modifications and alterations will occur to those skilled in the art. All such modifications and alterations are intended to fall within the scope of the appended claims.

C L A I M S

What is claimed is:

1. A personal computer system including means for importing and exporting color video signals and for providing digital video manipulation capability, comprising:

a) a microprocessor;

b) a main memory;

c) a raster-scanned video display;

d) means for receiving analog video signals at a real time rate;

e) means for digitizing the analog video signals for forming a digital signal having a plurality of color components, the means for digitizing including means for separating the color components;

f) means for compressing the digital signal at the real time rate for forming a compressed digital signal; and

g) means for storing the compressed digital signal.

2. The computer according to claim 1 wherein the means for storing further comprises:

a) a frame buffer for temporary storage of the compressed digital signal; and

b) a mass storage subsystem wherein the compressed digital signal is stored at the real time rate.

3. The computer according to claim 2 further comprising means for decompressing the compressed digital signal at the real time rate for forming a decompressed digital signal.

4. The computer according to claim 3 the decompressed digital is temporarily stored in the frame buffer.

5. The computer according to claim 1 further comprising:

a) means for receiving an analog audio signal;

b) means for digitizing the analog audio signal for forming a digital audio signal; and

c) means for storing the digital audio signal, wherein said audio input can operate concurrently with said video input.

6. The computer according to claim 5 further comprising:

a) means for compressing the digital audio signal prior to storing it for forming a stored compressed digital audio signal;

b) means for decompressing the stored compressed digital audio signal for forming a decompressed audio signal;

c) means for converting the decompressed audio signal into a converted audio signal; and

d) means for transmitting the converted audio analog signal.

7. The computer according to claim 6 wherein two channels of audio can be simultaneously received and further wherein two channels of audio can be simultaneously transmitted.

8. The computer according to claim 1 wherein the color video signals can be selected from the group of NTSC, PAL, or S-VHS formats.

9. A plug-in video board for a personal computer system capable of importing and exporting analog color video signals to the system, comprising:

a) means for electronically interfacing to the personal computer;

b) means for receiving an analog video signal including means for digitizing the analog video signal for forming a digital video signal;

c) means for compressing the digital video signal for forming a compressed digital video signal at a real time rate;

d) a frame buffer for storing digital compressed video;

e) means for retrieving stored compressed digital video signal forming a retrieved signal;

f) means for decompressing the retrieved signal for forming a decompressed signal; and

g) means for altering a decompressed signal.

10. The computer according to claim 9 further comprising a mass storage subsystem for storing the compressed digital signal is stored at the real time rate.

11. The computer according to claim 10 the decompressed signal is temporarily stored in the frame buffer.

12. The computer according to claim 9 further comprising:

a) means for receiving an analog audio signal;

b) means for digitizing the analog audio signal for forming a digital audio signal; and

c) means for storing the digital audio signal,

wherein said audio input can operate concurrently with said video input.

13. The computer according to claim 12 further comprising:

a) means for compressing the digital audio signal prior to storing it for forming a stored compressed digital audio signal;

b) means for decompressing the stored compressed digital audio signal for forming a decompressed audio signal;

c) means for converting the decompressed audio signal into a converted audio signal; and

d) means for transmitting the converted audio analog signal.

14. The computer according to claim 13 wherein two channels of audio can be simultaneously received and further wherein two channels of audio can be simultaneously transmitted.

15. The computer according to claim 9 wherein the color video signals can be selected from the group of NTSC, PAL, or S-VHS formats.

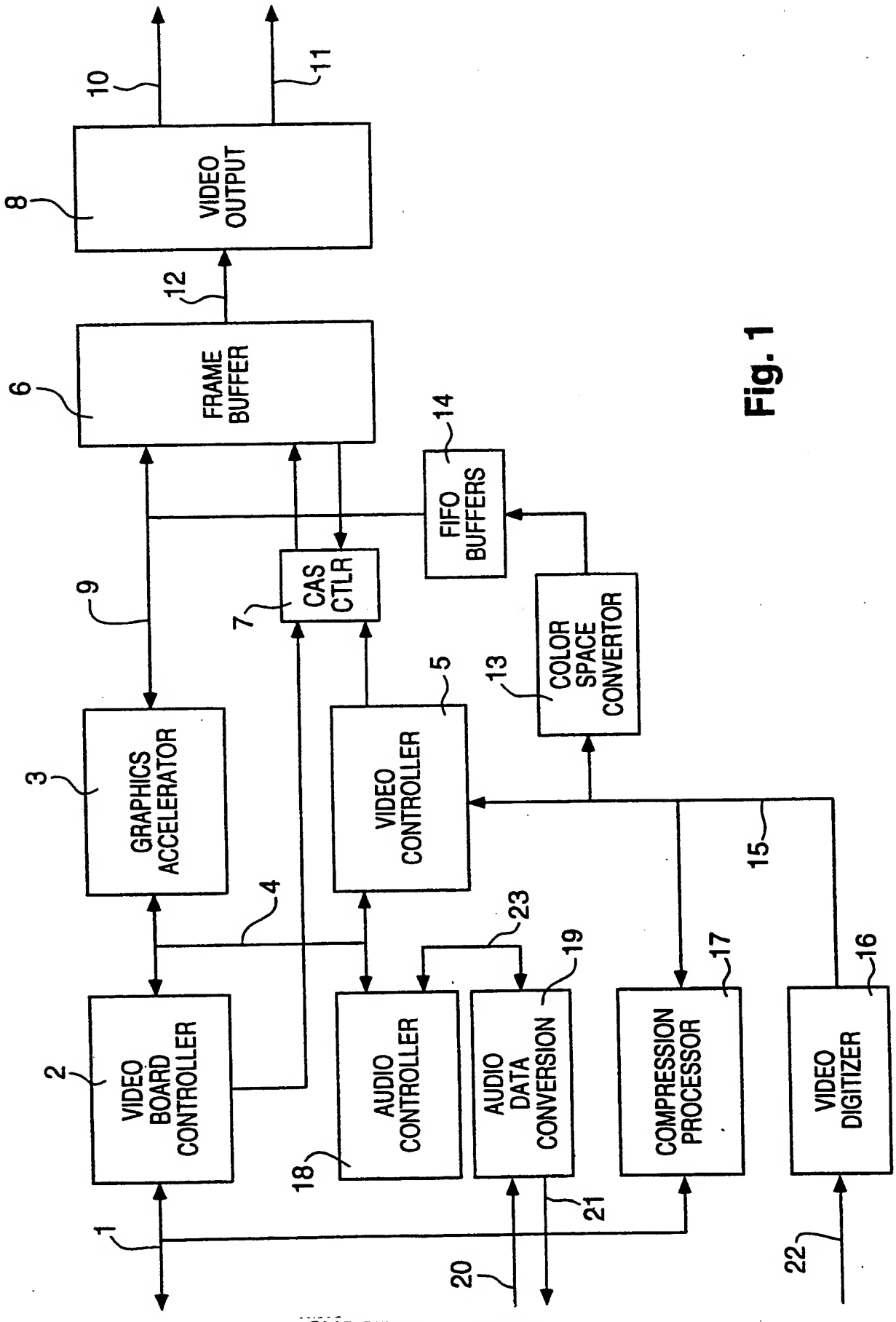
VIDEO OUTPUT
FRAME BUFFER
FIFO BUFFERS
CAS CTLR
COLOR SPACE CONVERTOR
GRAPHICS ACCELERATOR
VIDEO CONTROLLER
VIDEO BOARD CONTROLLER
AUDIO CONTROLLER
AUDIO DATA CONVERSION
COMPRESSION PROCESSOR
VIDEO DIGITIZER
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23

Fig. 1

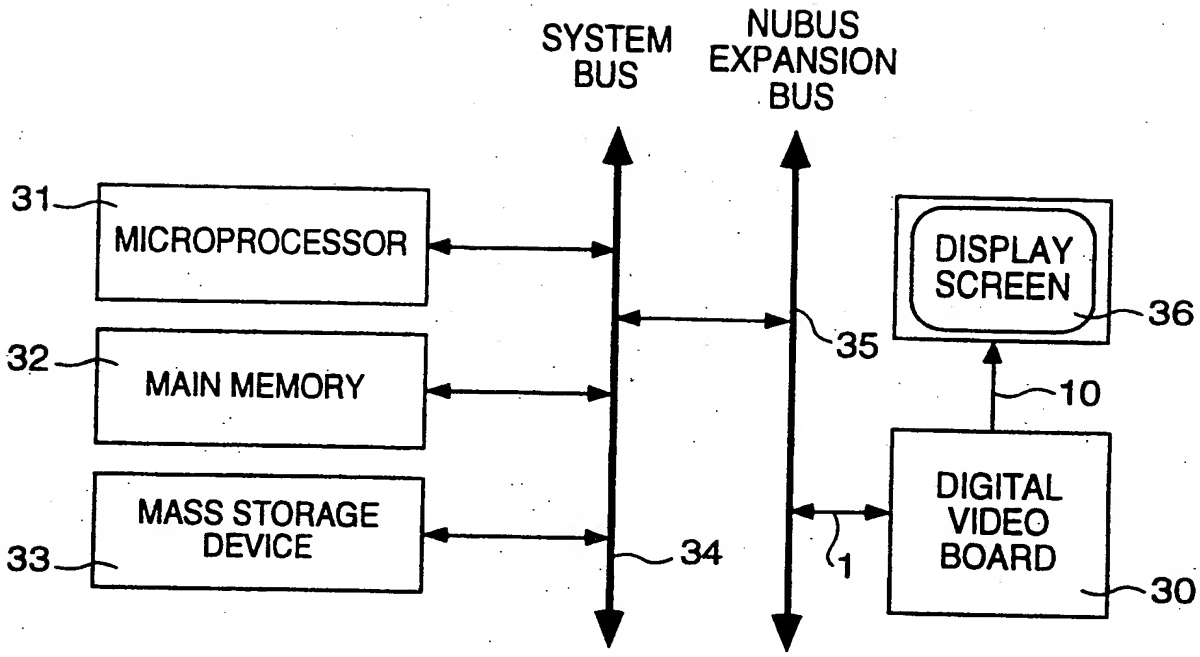
SYSTEM BUS
NUBUS EXPANSION BUS
31
MICROPROCESSOR
32
MAIN MEMORY
33
MASS STORAGE DEVICE
34
35
DISPLAY SCREEN
36
10
DIGITAL VIDEO BOARD
30
1

Fig. 2

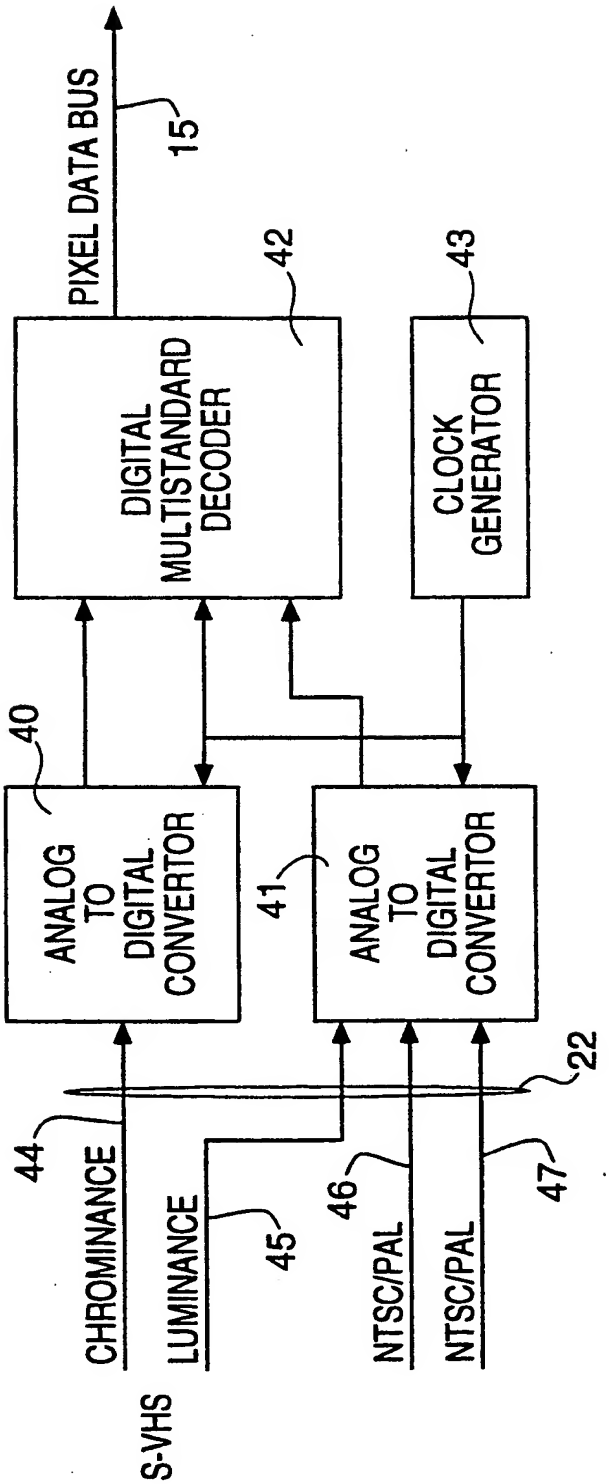
PIXEL DATA BUS
15
42
43
DIGITAL MULTISTANDARD DECODER
CLOCK GENERATOR
40
41
ANALOG TO DIGITAL CONVERTOR
ANALOG TO DIGITAL CONVERTOR
22
44
45
46
47
CHROMINANCE
LUMINANCE
NTSC/PAL
NTSC/PAL
S-VHS

Fig. 3

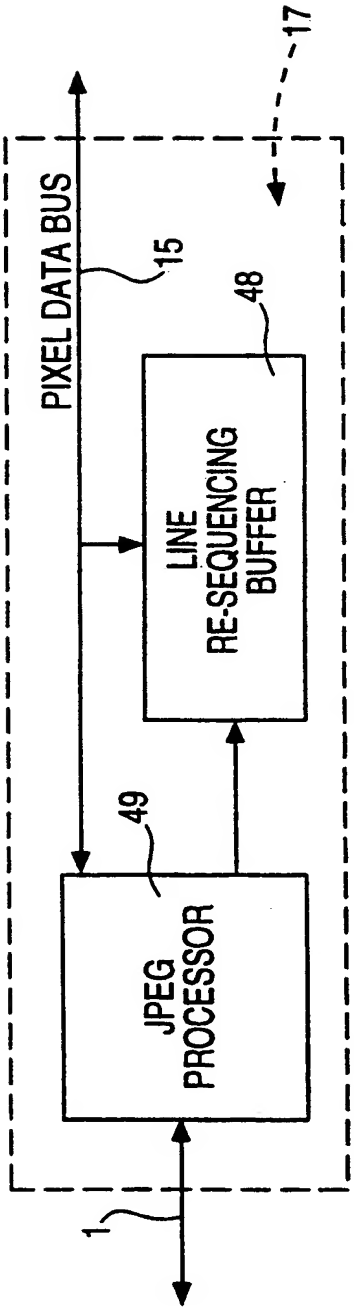
17
PIXEL DATA BUS
15
48
LINE RE-SEQUENCING BUFFER
49
JPEG PROCESSOR
1

Fig. 4

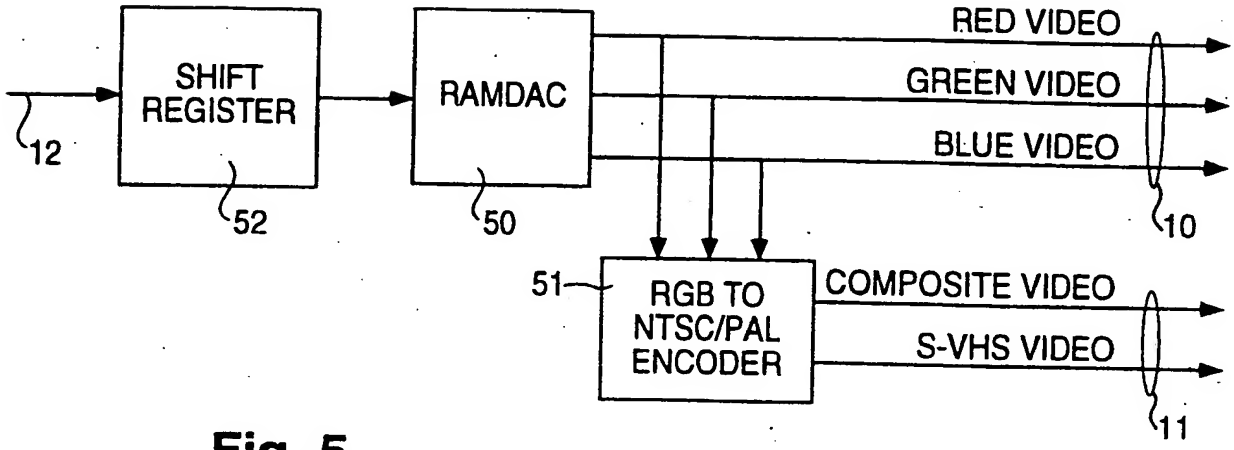
SHIFT REGISTER
12
52
RAMDAC
50
RED VIDEO
GREEN VIDEO
BLUE VIDEO
10
51
RGB TO NTSC/PAL ENCODER
COMPOSITE VIDEO
S-VHS VIDEO
11

Fig. 5

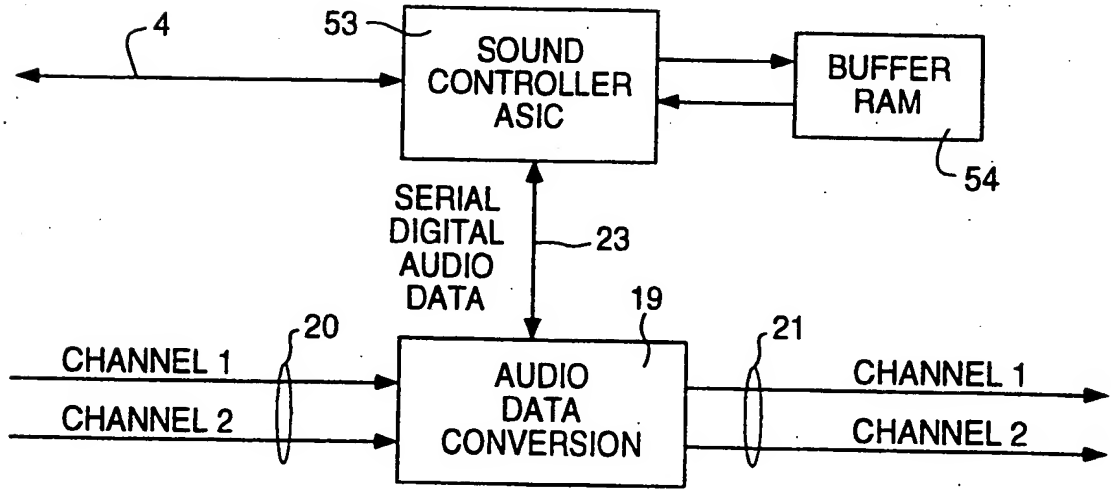
4
53
SOUND CONTROLLER ASIC
BUFFER RAM
54
SERIAL DIGITAL AUDIO DATA
23
19
20
21
CHANNEL 1
CHANNEL 2
AUDIO DATA CONVERSION
CHANNEL 1
CHANNEL 2

Fig. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US92/05560

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :G06F 3/00, 3/14
US CL :395/800; 358/133
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/800; 358/133; 364/514

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim
X	US, A, 4,951,139 (Hamilton et al) 21 August 1990, col. 4, line 11 - col. 10, line 7.	1-15
Y	US, A, 4,417,276 (Bennett et al) 22 November 1983, col. 1, line 62 - col. 2, line 18.	1,2,9
A,E	US, A, 5,132,992 (Yurt et al) 21 July 1992, Figure 2a.	1-15
A	US, A, 4,868,653 (Golin et al) 19 September 1989, Figures 1 and 2.	1,9
A	US, A, 4,849,807 (Music et al) 18 July 1989, Abstract, col. 2, line 32 - col. 3, line 25.	1,9
Y,P	US, A, 5,057,932 (Lang) 15 October 1991, Figures 2 - 4, col. 4, line 29 - col. 8, line 59.	1-15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or prior date and not in conflict with the application but cited to understand t principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot considered novel or cannot be considered to involve an inventive st when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot considered to involve an inventive step when the document combined with one or more other such documents, such combinati being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 10 AUGUST 1992	Date of mailing of the international search report 14 OCT 1992
Name and mailing address of the ISA/ Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer PAUL HARRITY Telephone No. (703) 308-4463

Form PCT/ISA/210 (second sheet)(July 1992)*